

WE CLAIM:

1 1. A varactor comprising:
2 a silicon layer;
3 a P- well in the silicon layer;
4 first and second N+ regions in the silicon
5 layer, wherein the first N+ region forms a first N+/P-
6 junction with the P- well, and wherein the second N+
7 region forms a second N+/P- junction with the P- well;
8 a gate oxide above the P- well; and,
9 a silicon gate above the gate oxide.

1 2. The varactor of claim 1 wherein the
2 silicon gate comprises a polysilicon gate.

1 3. The varactor of claim 1 wherein the
2 silicon layer is formed over an insulation layer so that
3 the silicon layer and the insulation layer together form
4 an SOI structure.

1 4. The varactor of claim 3 wherein the
2 insulation layer is formed over a layer of high
3 resistivity silicon.

1 5. The varactor of claim 1 wherein the
2 silicon layer is formed from bulk silicon.

1 6. The varactor of claim 1 wherein the
2 silicon layer is formed over a sapphire layer so that the
3 silicon layer and the sapphire layer together form an SOS
4 structure.

1 7. The varactor of claim 1 wherein the P-
2 well forms a transistor body, and wherein the transistor
3 body is allowed to float.

1 8. The varactor of claim 1 wherein the gate
2 silicon has a width to length ratio of approximately 16
3 to 1.

1 9. The varactor of claim 1 further comprising
2 a first metallization coupled to the gate silicon and a
3 second metallization coupled to the N+ regions.

1 10. The varactor of claim 1 wherein the first
2 and second N+/P- junctions extend from a top surface to a
3 bottom surface of the silicon layer.

1 11. A varactor comprising:
2 silicon layer;

3 a plurality of alternating P- wells and N+
4 regions in the silicon layer, wherein each P- well forms
5 a first N+/P- junction with the N+ region on one side of
6 the P- well and a second N+/P- junction with the N+
7 region on the other side of the P- well;
8 a gate oxide above each of the P- wells; and,
9 a silicon gate above each of the gate oxides.

1 12. The varactor of claim 11 wherein the
2 silicon gate above each of the gate oxides comprises a
3 polysilicon gate above each of the gate oxides.

1 13. The varactor of claim 11 wherein the
2 silicon layer is formed over an insulation layer so that
3 the silicon layer and the insulation layer together form
4 an SOI structure.

1 14. The varactor of claim 13 wherein the
2 insulation layer is formed over a layer of high
3 resistivity silicon.

1 15. The varactor of claim 11 wherein the
2 silicon layer is formed from bulk silicon.

1 16. The varactor of claim 11 wherein the
2 silicon layer is formed over a sapphire layer so that the
3 silicon layer and the sapphire layer together form an SOS
4 structure.

1 17. The varactor of claim 11 wherein the P-
2 wells form a transistor body, and wherein the transistor
3 body is allowed to float.

1 18. The varactor of claim 11 wherein each of
2 the gate silicons has a width to length ratio of
3 approximately 16 to 1.

1 19. The varactor of claim 11 further
2 comprising a first metallization coupled to the silicon
3 gate above each of the gate oxides and a second
4 metallization coupled to each of the N+ regions.

1 20. The varactor of claim 11 wherein each of
2 the N+/P- junctions extends from a top surface to a
3 bottom surface of the silicon layer.

1 21. A method comprising:
2 forming a plurality of alternating P- wells and
3 N+ regions in a silicon layer such that each P- well

4 forms a first N+/P- junction with the N+ region on one
5 side and a second N+/P- junction with the N+ region on
6 the other side;

7 forming a plurality of gate oxides, wherein
8 each of the gate oxides is formed above a corresponding
9 one of the P- wells;

10 forming a plurality of silicon gates, wherein
11 each of the silicon gates is formed above a corresponding
12 one of the gate oxides;

13 electrically coupling each of the silicon gates
14 together; and,

15 electrically coupling each of the N+ regions
16 together.

1 22. The method of claim 21 wherein each of the
2 silicon gates comprises a polysilicon gate.

1 23. The method of claim 21 further comprising
2 forming the silicon layer over an insulation layer so
3 that the silicon layer and the insulation layer together
4 form an SOI structure.

1 24. The method of claim 23 further comprising
2 forming the insulation layer over a layer of high
3 resistivity silicon.

1 25. The method of claim 21 wherein the silicon
2 layer comprises a bulk silicon layer.

1 26. The method of claim 21 further comprising
2 forming the silicon layer over a sapphire layer so that
3 the silicon layer and the sapphire layer together form an
4 SOS structure.

1 27. The method of claim 21 wherein the P-
2 wells form a transistor body, and wherein the transistor
3 body is allowed to float.

1 28. The method of claim 21 wherein each of the
2 silicon gates is formed so as to have a width to length
3 ratio of approximately 16 to 1.

1 29. The method of claim 21 wherein each of the
2 N+/P- junctions extends from a top surface to a bottom
3 surface of the silicon layer.

1 30. A varactor formed by a MOS transistor
2 structure and having a capacitive switching ratio equal
3 to or greater than 5.

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